REMARKS/ARGUMENTS

Claims 47 and 56 have been amended, and claims 60-65 have been canceled. (The amendments to claim 47 were to make the claim more readable and not for patentability reasons.) In addition, claims 66-72 are newly added. Claims 47-59 and 66-72 are now pending in the application. (Claims 1-46 were previously canceled.) Applicants respectfully request reexamination and reconsideration of the application.

As requested, the specification has been amended to update the status of parent applications.

Applicants note that this patent application claims priority as a divisional or continuation of the following applications: 09/468,620 (priority date 12/21/1999), 08/839,771 (priority date 4/15/1997), and 08/558,332 (priority date 11/15/1995). This application claims priority as a continuation-in-part of the following applications: 08/452,255 (priority date 5/26/1995), 08/340,144 (priority date 11/15/1994), 08/152, 812 (priority date 11/16/1993), 08/526,246 (priority date 9/21/1995), 08/533,584 (priority date 10/18/1995), and 08/554,902 (priority date 11/9/1995).

Claims 47-52 and 56-59 were rejected under 35 USC § 102(e) as anticipated by US Patent No. 5,532,610 to Tsujide et al. ("Tsujide"). In addition, claims 56 and 57 were rejected under 35 USC § 103(a) as obvious in view of Tsujide and US Patent No. 4,766,371 to Moriya ("Moriya"), and claims 53-55 were rejected under 35 USC § 103(a) as obvious in view of Tsujide and US Patent No. 4,945,302 to Janum ("Janum"). Applicants respectfully traverse these rejections.

Before discussing the specific claims pending in this application, it may be helpful to provide some background. As is known, semiconductor devices (e.g., dies) are typically manufactured many at a time on a semiconductor wafer. The devices are typically subjected to testing before being sold or used in a final product. Burn in—which involves heating the devices for a period of time—accelerates the appearance of latent defects and is typically performed after the devices are singulated from the wafer and packaged. Wafer-level burn in—which involves burning in the devices while the devices are still in wafer form—has long been a goal of the semiconductor testing industry. This is because burning in the devices before they are singulated and packaged saves the time and cost of packaging and otherwise processing bad devices.

Tsujide describes in more detail many of the benefits of wafer-level burn in. (Tsujide col. 1, line 7 through col. 2, line 22.)

Despite its many benefits, wafer-level burn in is not widely practiced due to several practical difficulties. Applicants' invention presents a novel approach to the implementation of wafer-level burn in.

In independent claim 47, resilient contact structures attached to terminals of the semiconductor devices of an unsingulated wafer is a key advancement toward effective and practical wafer-level burn in. Because the contact structures are resilient (i.e., spring-like), a burn in test board need only be pressed against the resilient contact structures in order to make temporary, pressure based electrical connections with the semiconductor devices. Moreover, because the resilient contact structures are attached to the semiconductor devices, the resilient contact structures can later be used to connect the singulated devices (after burn in and testing) to their final applications.

Tsujide—which is directed to wafer-level burn in of semiconductor dies—takes a very different approach to wafer-level burn in. In Tsujide, no resilient contact structures are attached to the terminals 3 of the dies of the wafer 1 being tested. Indeed, nothing is attached to the die terminals 3. Conductive layers 5 form part of the pad 4 attached to the testing substrate 2—not the wafer being tested 1. (Tsujide col. 4, lines 44-51 ("pads 4 which have anisotropic conductive layers 5 ***provided thereon***").) Tsujide therefore lacks a key feature of claim 47: an unsingulated semiconductor wafer with resilient contact structures attached to the terminals of the semiconductor devices of the wafer.

Moreover, nothing in Tsujide—or any of the other prior art of record—suggests attaching any type of contact structure, much less a resilient contact structure, to the die terminals 3 of the wafer being tested 1. In fact, Tsujide does not provide a teaching or even a hint that attaching resilient contact structures to the die terminals 3 would be desirable. In Moriya, elastic connectors 13 are not attached to the lead pins 6 of integrated circuit package 5. Rather, lead pins 6 are merely pressed against the elastic connectors 13 during testing of the integrated circuit package 5. Indeed, there would be no advantage or reason to attaching the elastic connectors 13 to the lead pins 6.

In short, Tsujide and Moriya do not teach or provide any suggestion or motivation to attach resilient contact structures to the terminals of semiconductor devices during wafer-level

burn in of the devices as described in claim 47. Independent claim 47 thus patentably distinguishes over Tsujide and any combination of Tsujide and Moriya.

Dependent claims 48-59 and 66-72 depend from claim 47 and are therefore also patentable. Moreover, claims 48-59 and 66-72 include additional features that further distinguish over the prior art of record. For example, claim 56 describes the resilient contact structures as free standing and attached to the terminals of the semiconductor devices. The Office Action seems to acknowledge that the elastic connectors 13 are neither free standing (i.e., able to stand on their own) nor attached to a device terminal while not compressed. (Office Action, pg. 3 ("***When compressed*** [the elastic connectors 13] are considered attached and free standing.") The mere act of compressing the elastic connectors 13, however, does not cause the connectors 13 to become attached to the lead pins 4 or change the connectors 13 from non-free standing structures to free standing structures. Indeed, if a structure is "free standing" only while compressed between two other entities, the structure is by definition not free standing. Claim 56 thus patentably distinguishes over the prior art of record. As other examples, new claims 66-72 recite additional features not taught or suggested by the prior art of record.

In view of the foregoing, Applicants submit that all of the claims are allowable and the application is in condition for allowance. If the Examiner believes that a discussion with Applicants' attorney would be helpful, the Examiner is invited to contact the undersigned at (801) 323-5934.

Respectfully submitted,

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By _____
N. Kenneth Burraston
Reg. No. 39,923

Kirton & McConkie
1800 Eagle Gate Tower
60 East South Temple
P.O. Box 45120
Salt Lake City, Utah 84111-1004
Telephone: (801) 323-5934
Fax: (801) 321-4893